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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,352	10/14/2003	George C. Valley	HRL 128	1230

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EXAMINER	
ALHIJA, SAIF A	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/22/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,352	VALLEY ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-42 have been presented for examination.

PRIORITY

2. Acknowledgment is made of applicant's claim for priority to provisional application #60/418044 filed on 12 October 2002.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 27 October 2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

MPEP 2106 recites:

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result" State Street 149 F.3d at 1373, 47 USPQ2d at 1601-02. A process that consists solely of the manipulation of an abstract idea is not concrete or tangibles. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed.Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459.

4. **Claims 1-42 are rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

i) The claims recite the steps of generating, selecting, and applying a model. As such the claims do not produce a useful, concrete, and tangible result.

ii) The claims are directed to a series of abstract mathematical steps such as generating matrices, selecting wavelets, and iteratively applying models. As such the claims do not produce a useful,

concrete, and tangible result.

iii) The claims appear to recite a computer program. It should be noted that code (i.e., a computer software program) does not do anything per se. Instead, it is the code stored on a computer that, *when executed*, instructs the computer to perform various functions. The following claim is a generic example of a proper computer program product claim;

A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

Function A
Function B
Function C, etc...

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of

each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claim(s) 1-42** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sangiovanni-Vincentelli "Design Methodologies for Analog and RF Integrated circuits"** hereafter referred to as **SV** in view of **Applicants own admission,** hereafter referred to as **AOA.**

6. **Claim(s) 1-42** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al. "Wavelet-Based Galerkin Method for Semiconductor Devices Simulation"** hereafter referred to as **Chang** in view of **Applicants own admission,** hereafter referred to as **AOA.**

Applicants own Admission in Paragraphs 6-7 of the Background, cited in the following rejection, states:

> [0006] Mixed-signal circuits, an example of which is the delta-sigma modulator, include both analog and digital functionality on the same chip and are difficult to simulate with conventional CAD software, such as SPICE or Simulink, for three main reasons: (1) they are described by a large number of equations; (2) the equations involve highly discontinuous non-linear operations at the clock period of the digital circuit; and (3) the equations are currently solved using slow, time-marching, algorithms (Runge-Kutta type).
>
> [0007] Recently, several approaches to fast simulation of mixed-signal circuits have been presented. Several are listed in the set of references below and are described here. Opal et al. presented a basic approach for circuits with a clock period in which linear differential equations are solved by one matrix multiply per clock cycle. In their method, a strong nonlinearity, such as the quantizer in a delta-sigma modulator, is simulated with a behavioral model at each clock period. Schreier and Zhang use a similar approach to construct recursion relations that update state variables of a delta-sigma modulator from time t to time $t+T_c$, where T_c represents the clock period. Cherry and Snelgrove compare three approaches: the recursion relation or direct integration approach, the time-marching method, and a z-domain extraction procedure, which were intended to combine the speed of the recurrence relations with the versatility of the time-marching method. Zhou et al., and Meliopoulos and Lee, have considered wavelet methods for use in general nonlinear circuit simulation and transient analysis.

Regarding Claim 1:

A method for simulating a mixed-signal system comprising acts of:

generating a matrix-based wavelet operator representation of equations characterizing a system, with the matrix-based wavelet operator representation including wavelet connection coefficients;

selecting a number of wavelets and a set of wavelet basis functions with which to represent a performance of the system, whereby the wavelet operator, the number of wavelets and the set of wavelet basis functions represent a wavelet model of the system;

and iteratively applying the wavelet model over a series of clock cycles to develop a behavioral model of the system.

(Claim Interpretation: The SV reference discloses behavioral modeling of mixed-signal systems in Section I, performance analysis in Section II, and the use of a Galerkin procedure, connection

coefficients, and system equations in Section IV-A to IV-B. The SV reference does not explicitly disclose the use of wavelets or applying a model over a series of clock cycles. Applicants own admission discloses the use of wavelets to characterize a system, as well as iteratively applying a model over a series of clock cycles to develop a behavioral model of a system, as well as independent selection for iteration which can be performed by SPICE/Simulink. See specifically, Paragraph 6, Lines 5-6 as well as Paragraph 7, Lines 4-9 and the last three lines.)

Applicants own admission and the SV reference are analogous art in that they deal with design/simulation of mixed-signal systems.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the wavelet and modeling methodologies discussed in **AOA** for the design/simulation methodologies in **SV** in order to allow for more "efficient system-level design methodologies" and the evaluation/design/simulation of mixed-signal circuits as discussed in the Abstract of **SV**.

(Claim Interpretation: The Chang reference discloses utilizing a wavelet-based Galerkin method for simulation of semiconductor devices. More specifically, the Chang Abstract, Introduction and Sections 3 and 5. The Chang reference does not explicitly disclose the use of clock cycles for iteration of the model. Applicants own admission discloses the use of wavelets to characterize a system, as well as iteratively applying a model over a series of clock cycles to develop a behavioral model of a system, as well as independent selection for iteration which can be performed by SPICE/Simulink. See specifically, Paragraph 6, Lines 5-6 as well as Paragraph 7, Lines 4-9 and the last three lines.)

Applicants own admission and the Chang reference are analogous art in that they deal with design/simulation of mixed-signal systems/semiconductor devices.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the wavelet and modeling methodologies discussed in **AOA** for the design/simulation methodologies in **Chang** in order to save computation time and provide for a more accurate result in the evaluation/design/simulation of semiconductor devices as discussed in the Abstract of **Chang**.

Regarding Claim 2:

The references disclose A method for simulating a mixed-signal system as set forth in claim 1, where the system is an electrical circuit.

(SV. Abstract)

(Chang. Title)

Regarding Claim 3:

The references disclose A method for simulating a mixed-signal system as set forth in claim 2, where the electrical circuit is a delta-sigma modulator. **(SV. A DSM is a type of mixed signal system discussed in the Abstract of SV)**

(Chang. A DSM is a type of semiconductor device as discussed in the Title and Abstract of Chang)

Regarding Claim 4:

The references disclose A method for simulating a mixed-signal system as set forth in claim 3, wherein in the generating act, the matrix-based wavelet operator is developed by a wavelet-Galerkin method. **(See rejection/citations for Claim 1)**

Regarding Claim 5:

SV discloses A method for simulating a mixed-signal system as set forth in claim 4, wherein in the generating act, the matrix-based wavelet operator is developed directly from a system diagram or from equations that describe the system. **(See rejection/citations for Claim 1)**

Regarding Claim 6:

SV discloses A method for simulating a mixed-signal system as set forth in claim 5, wherein in the selecting act the number of wavelets is selected independently for each iteration of the acts of the method. **(See rejection/citations for Claim 1)**

Regarding Claim 7:

SV discloses A method for simulating a mixed-signal system as set forth in claim 6, wherein in the selecting act, the set of wavelet basis functions is selected independently for each iteration of the acts of the method. **(See rejection/citations for Claim 1)**

Regarding Claim 8:

SV discloses A method for simulating a mixed-signal system as set forth in claim 7, further comprising acts of receiving a specification for a system model and outputting the behavioral model of the system. **(See rejection/citations for Claim 1)**

Regarding Claim 9:

SV discloses A method for simulating a mixed-signal system as set forth in claim 1, wherein in the generating act, the matrix-based wavelet operator is developed by a wavelet-Galerkin method. **(See rejection/citations for Claim 1)**

Regarding Claim 10:

SV discloses A method for simulating a mixed-signal system as set forth in claim 1, wherein in the generating act, the matrix-based wavelet operator is developed directly from a system diagram. **(See rejection/citations for Claim 1)**

Regarding Claim 11:

SV discloses A method for simulating a mixed-signal system as set forth in claim 1, wherein in the generating act, the matrix-based wavelet operator is developed directly from equations that describe the system. **(See rejection/citations for Claim 1)**

Regarding Claim 12:

SV discloses A method for simulating a mixed-signal system as set forth in claim 1, wherein in the selecting act the number of wavelets is selected independently for each iteration of the acts of the method. **(See rejection/citations for Claim 1)**

Regarding Claim 13:

SV discloses A method for simulating a mixed-signal system as set forth in claim 1, wherein in the selecting act, the set of wavelet basis functions is selected independently for each iteration of the acts of the method. **(See rejection/citations for Claim 1)**

Regarding Claim 14:

SV discloses A method for simulating a mixed-signal system as set forth in claim 1, further comprising acts of receiving a specification for a system model and outputting the behavioral model of the system. **(See rejection/citations for Claim 1)**

Regarding Claims 15-42:

See citations and rejections presented above for claims 1-14.

Conclusion

7. All Claims are rejected.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

December 18, 2006

KAMINI SHAH
SUPERVISORY PATENT EXAMINER